WHAT IS CLAIMED IS:

1. A method of performing a fast information compare within a processor comprising:

performing a more significant bit compare when information is loaded into a translation lookaside buffer, the more significant bit compare comparing more significant bits of the information being loaded into the translation lookaside buffer with more significant bits of compare information;

storing a result of the more significant bit compare within the translation lookaside buffer as part of an entry containing the information;

using the result of the more significant bit compare in conjunction with results from a compare of less significant bits of the information and less significant bits of compare information to determine whether a match is present.

2. The method of claim 1 further comprising:

providing an indication of a match to the compare information when the result of the more significant bit compare is active and the less significant bits of the information match the less significant bits of the compare information.

3. The method of claim 1 wherein:

the compare information corresponds to a virtual address watchpoint; and

the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to more significant bits of a watchpoint address.

4. The method of claim 1 wherein:

the compare information corresponds to sample selection criteria; and

the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to the sample selection criteria.

5. The method of claim 4 wherein:

the sample selection criteria includes a sample selection criteria low address, a sample selection criteria high address and sample selection criteria mid address; and

the result of the more significant bit compare indicates whether the more significant bits of the information being loaded correspond one of a plurality of conditions indicated by the sample selection criteria.

6. The method of claim 1 wherein:

the processor includes a memory management unit translation lookaside buffer and an instruction translation lookaside buffer; and

the more significant bit compare is performed when information is loaded into the instruction translation lookaside buffer.

7. The method of claim 1 wherein:

the processor includes a plurality of threads; and

the compare information is unique for each of the plurality of threads.

8. An apparatus for performing a fast information compare within a processor comprising:

means for performing a more significant bit compare when information is loaded into a translation lookaside buffer, the more significant bit compare comparing more significant bits of the information being loaded into the translation lookaside buffer with more significant bits of compare information;

means for storing a result of the more significant bit compare within the translation lookaside buffer as part of an entry containing the information;

means for using the result of the more significant bit compare in conjunction with results from a compare of less significant bits of the information and less significant bits of compare information to determine whether a match is present.

9. The apparatus of claim 8 further comprising:

means for providing an indication of a match to the compare information when the result of the more significant bit compare is active and the less significant bits of the information match the less significant bits of the compare information.

10. The apparatus of claim 8 wherein:

the compare information corresponds to a virtual address watchpoint; and

the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to more significant bits of a watchpoint address.

11. The apparatus of claim 8 wherein:

the compare information corresponds to sample selection criteria; and

the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to the sample selection criteria.

12. The apparatus of claim 11 wherein:

the sample selection criteria includes a sample selection criteria low address, a sample selection criteria high address and sample selection criteria mid address; and

the result of the more significant bit compare indicates whether the more significant bits of the information being loaded correspond one of a plurality of conditions indicated by the sample selection criteria.

13. The apparatus of claim 8 wherein:

the processor includes a memory management unit translation lookaside buffer and an instruction translation lookaside buffer; and

the more significant bit compare is performed when information is loaded into the instruction translation lookaside buffer.

14. The apparatus of claim 8 wherein:
the processor includes a plurality of threads; and
the compare information is unique for each of the plurality of threads.

15. A processor comprising:
a translation lookaside buffer; and
a first compare unit coupled to the translation lookaside buffer, the first compare unit performing a more significant bit compare when information is loaded into a translation lookaside buffer, the more significant bit compare comparing more significant bits of the information being loaded into the translation lookaside buffer with more significant bits of compare information, the first compare unit storing a result of the more significant bit compare within the translation lookaside buffer as part of an entry containing the information;
a second compare unit coupled to the translation lookaside buffer, the second compare unit processor using the result of the more significant bit compare in conjunction with results from a compare of less significant bits of the information and less significant bits of compare information to determine whether a match is present.

16. The processor of claim 15 wherein:
the second compare unit provides an indication of a match to the compare information when the result of the more significant bit compare is active and the less significant bits of the information match the less significant bits of the compare information.

17. The processor of claim 15 wherein:
the compare information corresponds to a virtual address watchpoint; and
the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to more significant bits of a watchpoint address.

18. The processor of claim 15 wherein:
the compare information corresponds to sample selection criteria; and
the result of the more significant bit compare indicates that the more significant bits of the information being loaded correspond to the sample selection criteria.

19. The processor of claim 18 wherein:
the sample selection criteria includes a sample selection criteria low address, a sample selection criteria high address and sample selection criteria mid address; and
the result of the more significant bit compare indicates whether the more significant bits of the information being loaded correspond one of a plurality of conditions indicated by the sample selection criteria.

20. The processor further comprising:
a memory management unit, the memory management unit including a memory management unit translation lookaside buffer; and
an instruction fetch unit, the instruction fetch unit including an instruction translation lookaside buffer, the more significant bit compare being performed when information is loaded into the instruction translation lookaside buffer.

21. The processor of claim 15 wherein:
the processor includes a plurality of threads; and
the compare information is unique for each of the plurality of threads.